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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,684	02/20/2004	Hai-Zhi Song	040070	3691

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/781,684	SONG, HAI-ZHI	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *12-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9 and 11* is/are rejected.

7)☒ Claim(s) *2,8 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 04/14/2005 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 5-7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 5 and 6 requires depletion region, claimed in claim 1 (from which claim 5 depends) line 13. Additionally these claims require a second set of depletion regions claimed line 3 of claim 5. At the time the application was filed, the subject matter described in the specification only reasonably conveyed the applicant's possession of one set of depletion regions, not the additional depletion regions claimed in claim 5.

Claim 7 requires a gate electrode, claimed in claim 1 (from which claim 7 depends) line 9. Additionally claim 7 requires a second gate electrode claimed line 3 of claim 7. At

the time the application was filed, the subject matter described in the specification only reasonably conveyed the applicant's possession of one gate electrode, not the additional gate electrode claimed in claim 7.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1,3,4, and 9 rejected under 35 U.S.C. 102(e) as being anticipated by SHIELDS (6,720,589).

Shields discloses a quantum semiconductor device comprising a first semiconductor layer 81 formed over a substrate 71 and having a two-dimensional carrier gas (the 2DEG is part 47 in "close-up" figure 44a and seen as a line of +++'s in figure 45) formed in; a quantum dot 87b formed over the first semiconductor layer 81; a second semiconductor layer 88 formed over the first semiconductor layer 81, covering the quantum dot 87b; another quantum dot, forming a dot-shaped structure 87a formed on

the surface of the second semiconductor layer 88 at a position above the quantum dot 87b; a gate electrode 99 electrically connected to the dot-shaped structure 87a; source/drain regions (no part #'s, seen in figure 45 directly below source/drain electrodes 93 and 95) formed in the second semiconductor layer 88 on both sides of the quantum dot 87b and connected to both ends of the channel region; and oxide layers ("upper barrier" 109 form layers on the sides of each of a several dot-shaped structures 87a, see "close-up" in figure 42) formed on both sides of the dot-shaped structure 87a on the upper surface of the second semiconductor layer 88, wherein depletion regions (see column 20 lines 44-47) are formed in regions of the first semiconductor layer 81 which are below the oxide layers, and the depletion regions define a channel region (see column 20 lines 46-50). Note figures 42,44a-f, 45, column 20 lines 44-50, column 33 lines 12-26 and 61-67, column 34 lines 1-17 and 45-67, and column 35 lines 1-17.

The applicant's claims 3 and 4 do not distinguish over the Shields reference regardless of the process used to form the quantum dot and dot-shaped structure, because only the final product is relevant, not the recited processes of self-assembling the quantum dot and the dot-shaped structure by S-K mode.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal

with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

B. Claim 11 stands rejected under 35 U.S.C. 102(b) as being anticipated by JAIN ET AL. (6,498,360).

Jain et al. discloses a method of making said quantum semiconductor device comprising the steps of forming on a substrate 10 a first semiconductor layer 20 with a two-dimensional carrier gas 19 formed in; forming a quantum dot 25 on the first semiconductor layer 20; forming a second semiconductor layer 24, covering the quantum dot 25; forming a dot-shaped structure 23 on the surface of the second semiconductor at a position above the quantum dot 25 due to strains generated in the surface of the second semiconductor layer 24 due to the presence of the quantum dot 25; and forming oxide layers 21 and 22 on both sides of the dot-shaped structure 23 on the upper surface of the second semiconductor layer 24. Note figures 2,8,9, column 3 lines 15-20,53-54, column 4 lines 17-20, and column 6 lines 25-29 and 53-54 of Jain et al.

Allowable Subject Matter

4. Claims 2,8, and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

1. Applicant's arguments with respect to claims 1,3,4, and 9 have been considered but are moot in view of the new ground(s) of rejection.

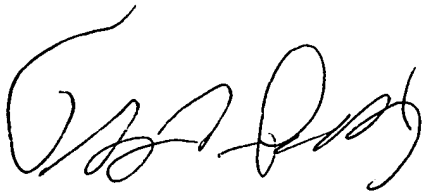
It is argued, at page 8 of the remarks, that "Jain [sic] fails to expressly or inherently describe the following features set forth in claim 11: 'forming a quantum dot over the first semiconductor layer; forming a second semiconductor layer, burying the quantum dot; forming a dot-shaped structure on the surface of the second semiconductor at a position above the quantum dot due to strains generated in the surface of the second semiconductor layer due to the presence of the quantum dot; and forming oxide layers on the upper surface of the second semiconductor layer on both side of the dot-shaped structure with the dot-shaped structure as a mark," in combination with the other claimed features." The examiner observes that there are no other features claimed in claim 11. Applicant has simply copied claim 11 and set it down in his remarks section.

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
06/06